REMARKS

The Examiner's Action mailed on June 30, 2005, has been received and its contents carefully considered. Additionally attached to this Amendment is a Petition for a One-month Extension of Time, extending the period for response to October 30, 2005, together with the requisite fee. Moreover, in order to ensure consideration of the changes to independent claim 1, submitted concurrently with this Amendment is a Request for Continued Examination, together with the necessary fee.

In this Amendment, Applicant has amended independent claim 1. Claim 1 is the only independent claim, and claims 1-10 and 21-26 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claims 1-10 and 21-26 as being obvious over *Noerholm* in view of *Marr*, *Whitney* and *Okada*. It is submitted that these claims are *prima facie* patentably distinguishable over the cited references, either taken alone or in any reasonable combination, for at least the following reasons.

Initially, it is noted that the Examiner's Action has not addressed claims 21-26, which claims were added with the Amendment filed on April 12, 2005. Although the Examiner's Action states that these claims are unpatentable in view of the cited references, the Examiner refers to the reasons presented in the previous Office Action. However, these claims were added in response to the rejections presented in the previous Office Action, and were therefore not

addressed within the previous Office Action. As such, it is submitted that the Examiner's Action has failed to provide a *prima facie* case of obviousness against at least claims 21-26.

Moreover, it is submitted that Applicant's independent claim 1 is patentably distinguishable over the cited references for at least the reason that this claim recites a semiconductor device which includes a semiconductor substrate and a fuse circuit disposed on the semiconductor substrate. The fuse circuit includes a first conductive region and a second conductive region, wherein the first conductive region has multi-layered structure and the second conductive region has a less layered structure than the first conductive region. Moreover, this claim recites that the first conductive region includes a plurality of conductive layers and a respective interlayer insulating layer disposed between respective adjacent ones of the conductive layers. This claimed configuration thus provides for a fuse circuit that can be fabricated using a multi-layered structure, when a semiconductor integrated circuit is formed, without using additional elements. As such, the fuse circuit according to the present invention can be made at a lower cost.

In contrast, the primary reference to *Noerholm* only discloses a plurality of conductive lines, such as shown in figure 8, which are disposed directly on top of each other without any intervening insulating layers. Thus, not only does this reference not disclose or suggest a semiconductor device, but this reference likewise does not disclose or suggest a fuse circuit that is fabricated from a multi-

layered structure of a semiconductor integrated circuit, that is, a fuse circuit that has a first conductive region which includes a plurality of conductive layers and a respective interlayer insulating layer disposed between respective adjacent ones of the conductive layers. In fact, since this reference is not directed to a semiconductor substrate, one skilled in the art would have had no motivation to have provided an interlayer insulating layer between the various conductive layers, such as layers 20, 21, and 22 shown in figure 8 of the cited reference, except in a hindsight attempt at reconstructing Applicant's claimed invention. Thus, since the primary reference does not disclose or suggest Applicant's claimed semiconductor device having a fuse circuit which has a first conductive region as recited within claim 1, and since the cited references fail to provide any motivation to modify the primary reference in a manner that would render Applicant's claimed invention obvious, it is submitted that Applicant's independent claim 1, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited references. As such, it is requested that these rejections be withdrawn and that these claims be allowed.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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